IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Georg Braun et al.

Serial No.: 10/777,992

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For: METHOD AND CIRCUIT FOR ALLOCATING MEMORY ARRANGEMENT ADDRESSES

§

Group Art Unit: 2186

Examiner: Paul W. Schlie

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

CERTIFICATE OF MAILING OR TRANSMISSION

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June 20, 2006 _____
Date Joseph Jong

RESPONSE TO OFFICE ACTION DATED MARCH 20, 2006

In response to the Office Action dated March 20, 2006, having a shortened statutory period for response set to expire on June 20, 2006, please enter this response and reconsider the claims pending in the application for reasons discussed below. While no fees are believed due, the Commissioner is hereby authorized to charge counsel's Deposit Account No. 20-0782/INFN/WB0059/GGM for any fees, including extension of time fees or excess claim fees, required to make this response timely and acceptable to the Office.

The Claims are reflected in the listing of claims which begins on page 2 of this paper. Remarks/Arguments begin on page 6 of this paper.

IN THE CLAIMS:

The claims remain as follows:

1. (Original) A method for allocating memory arrangement addresses to a buffer chip, during an initialization mode, for use in addressing one or more memory arrangements connected to the buffer chip, comprising:

receiving first initialization data specifying a first set of available memory arrangement addresses;

associating one or more of the first set of available memory arrangement addresses with the one or more memory arrangements connected to the buffer chip;

generating second initialization data specifying a second set of available memory arrangement addresses comprising the first set of available memory arrangement addresses less the memory arrangement addresses associated with the one or more memory arrangements connected with the buffer chip; and

transmitting the second initialization data from the buffer chip.

2. (Original) The method of claim 1, wherein the first initialization data comprise a number of bits, with each bit corresponding to an address for a memory arrangement.

3. (Original) The method of claim 1, wherein:

the initialization mode is entered after at least one of: reset or power-up of the buffer chip; and

the initialization mode is terminated after the memory arrangement addresses have been allocated.

4. (Original) The method of claim 3, wherein reset or power-up of the buffer chip is followed by an arbitrary memory arrangement address being allocated, so that the command data sent to the arbitrary memory arrangement address is received by the buffer chip .

5. (Original) The method of claim 1, wherein the initialization mode is entered in response to command data being received.

6. (Original) The method of claim 1, wherein, in a normal mode, the buffer chip receives data and forwards them in parallel to the one or more memory arrangements, receives the data from the one or more memory arrangements and transmits them serially, or both.

7. (Original) The method of claim 1, wherein transmitting the second initialization data from the buffer chip comprises transmitting the second initialization data to another buffer chip for use in allocating memory arrangement addresses to memory arrangements connected thereto.

8. (Original) The method of claim 7, wherein the buffer chips are connected in series such that a first buffer chip transmits the second initialization data in the form of first initialization data to a second buffer chip.

9. (Original) The method of claim 8, wherein the first buffer chip receives the first initialization data from a memory access control unit.

10. (Original) The method of claim 8, wherein the second buffer chip transmits the second initialization data to a memory access control unit.

11. (Original) A buffer chip for use with one or more memory arrangements, comprising:

a reception unit for receiving first initialization data which specify available memory arrangement addresses;

a transmission unit for transmitting second initialization data; and

an initialization unit for, during an initialization mode, associating memory arrangement addresses with the one or more memory arrangements, the associated memory arrangement addresses being chosen from the available memory arrangement

addresses, wherein the initialization unit generates second initialization data specifying the memory arrangement addresses which are still available after the association.

12. (Original) The buffer chip of claim 11, further comprising a conversion unit which has a parallelization unit for parallelizing received data and has a serialization unit for serializing data which are to be transmitted.

13. (Original) The buffer chip of claim 11, wherein the initialization unit enters the initialization mode after the buffer chip in response to at least one of: reset or power-up of the buffer chip.

14. (Original) The buffer chip of claim 11, wherein the initialization unit enters the initialization mode after command data have been received.

15. (Original) A memory module comprising:

one or more memory arrangements; and

a buffer chip coupled with one or more memory arrangements, wherein the buffer chip comprises a reception unit for receiving first initialization data which specify available memory arrangement addresses, an initialization unit for, during an initialization mode, associating one or more of the available memory arrangement addresses with the one or more memory arrangements and generating second initialization data specifying the memory arrangement addresses which are still available after the association, and a transmission unit for transmitting the second initialization data.

16. (Original) The memory module of claim 15, wherein the memory module is in the form of a DIMM module.

17. (Original) A memory system comprising:

a memory access control unit; and

one or more memory modules, each comprising one or more memory arrangements and a buffer chip coupled with one or more memory arrangements, wherein the buffer chip comprises a reception unit for receiving first initialization data which specify available memory arrangement addresses, an initialization unit for, during an initialization mode, associating one or more of the available memory arrangement addresses with the one or more memory arrangements and generating second initialization data specifying the memory arrangement addresses which are still available after the association, and a transmission unit for transmitting the second initialization data.

18. (Original) The memory system of claim 17, wherein a buffer chip of a first one of the memory modules receives first initialization data from the memory access control unit.

19. (Original) The memory system of claim 18, wherein a buffer chip of a last one of the memory modules transmits second initialization data to the memory access control unit.

20. (Original) The memory system of claim 17, wherein the buffer chips enter the initialization mode in response to at least one of: reset of the memory modules, power-up of the memory modules, and command data.

REMARKS

This is intended as a full and complete response to the Office Action dated March 20, 2006, having a shortened statutory period for response set to expire on June 20, 2006. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-20 are pending in the application. Claims 1-20 remain pending following entry of this response.

Claim Rejections - 35 USC § 112

Claims 1-20 are rejected under 35 U.S.C. 112, first paragraph, for lack of enablement. Applicants respectfully traverse the rejection, first reviewing the Examiner's argument and the enablement requirements, and then responding to the Examiner's argument.

The Examiner's Argument

The Examiner states that the specification does not enable the information necessary for coherent DRAM access control, such as bank configuration or row/column organization of each of the said modules, to be communicated back to the controller. The Examiner states that such information is necessary for access per the control signals depicted within Figure 2, and within the body of the disclosure.

35 U.S.C. § 112 ¶ 1 Enablement Requirements

35 U.S.C. § 112 ¶ 1 states that the specification shall contain the manner and process of making and using the claimed invention, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which the claimed invention pertains to make and use the claimed invention. The test of enablement is whether one reasonably skilled in the art could make or use the claimed invention from the disclosures in the patent coupled with information known in the art without undue experimentation. *See* MPEP § 2164.01, citing *United States v. Telectronics*, 857 F.2d 778, 785 (Fed. Cir. 1988). However, it is well-settled that the enablement requirement does not require a patent to teach, and preferably omits, what is well known in the art.

See id., citing *In re Buchner,* 929 F.2d 660, 661 (Fed. Cir. 1991). The amount of guidance or direction needed to enable the claimed invention is inversely related to the amount of knowledge in the state of the art as well as the predictability of the art. *See* MPEP § 2164.03. Finally, Examiner has the initial burden to establish a reasonable basis to question the enablement provided for the claimed invention. *See* MPEP § 2164.04. Any conclusion of nonenablement must be based on the evidence as a whole. *See* MPEP § 2164.01(a) citing *In re Wands,* 858 F.2d 731, 737 (Fed. Cir. 1988). Specifically, Examiner must consider all of the evidence related to each of the factors presented by *In re Wands*. *See id.*

Response to Examiner's Enablement Arguments

Applicants respectfully submit that Examiner has not established the factors required to prove nonenablement. First, Examiner has not established the level of one of ordinary skill in the art. Further, Examiner has not discussed the level of predictability in the art. Also, Examiner has not considered information known in the art.

The Examiner's arguments appear to be directed to enablement with respect to "DRAM access control" information being transmitted to a memory controller. Applicants submit that general DRAM access control (*e.g.,* reading data from and writing data to a DRAM) is well known in the art. Accordingly, Applicants respectfully submit that, with respect to the Examiner's suggested reasons for nonenablement, a person of ordinary skill in the art would be able to make and use the claimed invention. Withdrawal of the rejection is respectfully requested.

Claim Rejections - 35 U.S.C. § 103

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over David (6,931,505) in further in view of Sathaye et al. (5,517,617). Applicants respectfully traverse this rejection.

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one ordinary skill

in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP § 2143. The present rejection fails to establish at least the first and third criteria, as described below.

With respect to the third criteria of the *prima facie* case of obviousness, the pending claims describe, for example, generating second initialization data specifying a second set of available memory arrangement addresses comprising the first set of available memory arrangement addresses less the memory arrangement addresses associated with the one or more memory arrangements connected with the buffer chip. The Examiner states that *Sathaye* describe the claimed subject matter in the Abstract at lines 9-14, stating that *Sathaye* teaches a controller which may derive its address as a function of it's neighbor's so initialized address.

Applicants first note that the Abstract of *Sathaye* does not specifically refer a to controller. Also, the Abstract states that an apparatus is responsive for configuring an address of the apparatus from a neighbor address. The Abstract does not refer to a set of available addresses, nor does the abstract describe that any addresses are associated with one or more memory arrangements connected with a buffer chip. Thus, the Abstract of *Sathaye* does not describe "generating second initialization data specifying a second set of available memory arrangement addresses comprising the first set of available memory arrangement addresses less the memory arrangement addresses associated with the one or more memory arrangements connected with the buffer chip". Accordingly, withdrawal of the rejection is respectfully requested.

With respect to the first criteria of the *prima facie* case of obviousness, the Examiner states that it would have been obvious to combine *David* and *Sathaye* to enable a memory module to receive an initialize command from its neighbor including its initialized address range. First, Applicants note that, as described above, *Sathaye* does not describe initializing an address range as asserted by the Examiner.

Furthermore, Applicants note that *David* is directed generally to memory modules within a computer system memory subsystem. *See David*, Col. 1, Lines 12-14. The memory modules are connected to a memory controller within a computer system and

are interconnected by an internal point-to-point interconnect. Thus, *David* is directed to sub-components within a memory subsystem which is a further sub-component of a computer system. In contrast, *Sathaye* is directed to communication between separate computers on a computer network (*e.g.,* an ATM network) as described in *Sathaye* at Col. 1, Lines 14-28 and Col. 1, Lines 60-62.

Applicants submit that a person of ordinary skill in the art would not be motivated to combine the teachings of *David* regarding computer memory subsystems within a computer with the teachings of *Sathaye* regarding inter-computer communication in a computer network. Neither reference suggests such a combination, and furthermore, a person skilled in the art of computer memory subsystems (*e.g.,* as described in *David*) would not be motivated to combine teachings from *Sathaye* regarding communication between separate computers in a network (*e.g.,* as described in *Sathaye*) because the issues associated with network communication between separate computers are inapposite to the issues associated with computer memory subsystems. Furthermore, because the teachings of *David* and *Sathaye* are inapposite to one another, Applicants also submit that the references are non-analogous art and therefore cannot be combined in an obviousness rejection under 35 USC Sec. 103(a). *See* MPEP Sec. 2141.01(a). Accordingly, Applicants submit that there is no motivation to combine the references as asserted by the Examiner. Accordingly, withdrawal of the rejection is respectfully requested.

Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Conclusion

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

/Gero G. McClellan, Reg. No. 44,227/
Gero G. McClellan
Registration No. 44,227
PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Applicants